## REMARKS

The Applicant hereby traverses the rejections of record and requests reconsideration and withdrawal of such in view of the remarks herein. Claim 23 has been amended to correct a typographical error. Claims 1-23 are pending in this application.

**Rejection under 35 U.S.C. § 102 (Walton)**

Claims 15-20 and 23 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 7,103,639 to Walton et al. (hereinafter Walton).

It is well settled that to anticipate a claim, the reference must teach every element of the claim, see M.P.E.P. § 2131. Moreover, in order for a prior art reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he elements must be arranged as required by the claim," see M.P.E.P. § 2131, citing In re Bond, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). Furthermore, in order for a prior art reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim," see M.P.E.P. § 2131, citing Richardson v. Suzuki Motor Co., 9 U.S.P.Q.2d 1913 (Fed. Cir. 1989). Applicants respectfully assert that the rejection does not satisfy these requirements.

Claims 15-20

Claim 15 requires, in part, firmware comprising a reset code that resets a portion of the partition, wherein one processor of the plurality of processors executes the reset code, and random access memory that is not affected by the reset code, that stores a list of addresses associated with the portion. Walton does not describe at least these limitations.

Walton describes a system for managing the formation of a partition from a plurality of independent cells. Abstract. Specifically, Walton describes configuration activities that occur to transition from having individual cells acting independently, to having cells rendezvous and become interdependent to continue operations as a partition. Abstract. Individual cells may be reset if they contain the wrong configuration or cached values, or if the cells are not compatible with the partition or otherwise malfunction.

Walton does not ever describe the resetting of the partition or a portion of the partition as required by claims 15-20. The Examiner asserts that the monarch processor of Walton includes booting code which is inclusive of initialization and reset, citing column 3, lines 5-12 and column 5, lines 35-47. Applicant respectfully disagrees with the Examiner's characterization of the cited portions of Walton.

Column 3, lines 5-12 define a cell as including a processor dependent hardware (PDH) module which implements instructions executed on CPUs 302 pertaining to the formation of partitions. No mention is made of resetting a portion of a partition after it has been formed. Column 5, lines 35-47 describes a portion of Figure 2 which relates to "the partition formation process". Column 5, lines 35-36. The cited portion states that one processor of CPUs 302 is arbitrarily selected to manage the booting and partition formation activities associated with its respective cell. Column 5, lines 43-45. Again no mention is made of code for resetting a portion of a partition as required by claim 15.

While Walton is very detailed in its description of the partition formation process, Applicant can find no description in Walton of resetting a partition or portion of a partition as required in the rejected claims. Walton describes resetting individual cells that are rejected as part of the partition formation process (see, Figure 2), but that is not the same as a partition reset.

Claim 15 also requires random access memory that is not affected by the reset code, that stores a list of addresses associated with the portion. The Examiner also states that cell micro-controllers (CMs) 304 in each cell as meeting this limitation. The Examiner points to the complex configuration stored in each CM as meeting necessarily including a list of addresses. Applicant respectfully disagrees with the Examiner's characterization. Applicant can find no description in Walton of the CM that refers to a list of addresses for a portion of a partition being reset that is stored in the complex characterization of the CM. Even if each complex characterization stored a list of all the cells in a partition, this is not equivalent to a list of addresses associated with a portion of a partition being reset as required by claim 15.

As claim 15, and claims 16-20 through their dependency from claim 15, include limitations as described above that are not found in Walton. Claims 15-20 are allowable over the rejection of record.

Claim 23

Claim 23 requires means for building a list of reset register addresses associated with the plurality of processors, means for placing each processor of the plurality of processors into a known state, and means for resetting the plurality of processors by writing a reset code into their associated reset registers.

As described with respect to claim 15, Walton describes a partition formation process and mechanism, but does not disclose anything related to a means for resetting a plurality of processors by writing a reset code into their associated reset registers. The Examiner has referenced the BIB code described by Walton as meeting the limitation of a reset code. Applicant respectfully disagrees. The BIB, or boot inhibit bit, causes the boot process of a processor or cell to continue to a particular point. Column 4, lines 51-56. The boot inhibit bit may be used to enter a spin loop cycle until the boot inhibit bit is released by the service processor. Column 6, lines 7-11. As described by Walton, including those portion of Walton cited by the Examiner, the boot inhibit bit stops the boot process at specific states to allow for the rendezvous of cells in the partition formation process. The boot inhibit bit is not a reset code as required by claim 23.

As Walton does not describe each and every limitation of claim 23, Applicant asserts that claim 23 is allowable over the rejection of record.

**Rejection under 35 U.S.C. § 103 (Walton in view of Harrington)**

Claims 1-13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Walton in view of U.S. Patent Publication No. 2003/0236972 to Harrington et al. (hereinafter, "Harrington").

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art cited must teach or suggest all the claim limitations. *see* M.P.E.P.

§ 2143. Without admitting that the second criteria is satisfied, the Applicant respectfully asserts that the Examiner's rejection fails to satisfy the first or third criteria.

Lack of All Claim Limitations.

Claim 1 requires executing, by one processor of the plurality of processors, a reset code from firmware, building a list of reset register addresses associated with the plurality of processors, sending an interrupt to the other processors of the plurality of processors, resetting the other processors by writing a reset code to their associated reset registers, and resetting the one processor by writing to its associated reset register. The combination put forth by the Examiner does not describe these limitations.

The Examiner asserts that Walton booting code which is inclusive of initialization and reset (Office Action, page 4) citing the firmware code described at column 3, lines 5-12 and column 5, lines 35-47, and a list of reset register addresses citing to the complex profile described at column 2, lines 7-15 and column 4, line 47 through column 5, line 34. Harrington is not relied upon as describing these limitations. Applicant again respectfully disagrees with the Examiner's characterization of Walton.

As set forth with reference to claims 15 and 23, Walton describes a method and mechanism for forming partitions from multiple independent cells. Abstract. Walton, however is completely silent to resetting partitions or portions of partitions using a reset code from firmware. The only description of resetting is the resetting of individual cells, not partitions, when a cell does not meet some criteria as part of the partition formation process. See, Figure 2. Further, the description of the complex profile includes no description of a list of reset register addresses associated with the plurality of processors. If the Examiner is aware of details of the Walton device beyond that described in Walton, the Applicant respectfully request that the information be made of record and supplied to the Applicant.

As Walton does not describe, and Harrington is not relied upon as describing, the limitations set forth above, Applicant respectfully asserts that claims 1-13 are allowable over the rejection of record.

Lack of Motivation

The mere fact that references can be combined does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. see In re Mills, 916 F.2d 680 (Fed. Cir. 1990); M.P.E.P. § 2143. Applicant respectfully submits that neither Walton, nor Harrington provides motivation for the combination, as the Examiner suggests.

The Examiner's stated motivation for combining Harrington with Walton is "as doing so would give the added benefit of having a more reliable reboot process in a partition system ensuring all pending I/O requests within the system are halted/completed (as taught by Harrington above). As described by Applicant, Walton is completely silent as to resetting partitions or portions of partitions. As Walton is drawn to partition formation and not resetting and contains no description of partition resetting there is no motivation to combine Walton with Harrington to give Walton a "more reliable reboot process in a partition system" as asserted by the Examiner.

Applicant would respectfully assert that the suggestion to make the claimed combination and reasonable expectation of success must both be found in the prior art and not based on the Applicant's disclosure. M.P.E.P. 2142, citing In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). For the reasons set forth above Applicant respectfully asserts that there is no motivation to combine Harrington and Walton. Applicant, therefore, respectfully requests that the rejections based on the combination of Harrington and Walton be withdrawn.

**Rejections under 35 U.S.C. § 103 (Walton in view of Harrington and/or Admitted Prior Art)**

Claim 14 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Walton in view of Harrington and further in view of Applicant's Admitted Prior Art. Claim 21 is rejected as being unpatentable over Walton in view of Harrington. Claim 22 is rejected as being unpatentable over Walton in view of Applicant's Admitted Prior Art.

Claim 14 depends from claim 1 and therefore inherit all the limitations thereof. Claim 14, therefore, is allowable for at least the reasons set forth above with respect to claim 1. Claims 21 and 22 depend from claim 15 and therefore inherit all the limitations thereof. Claims 21 and 22, therefore, is allowable for at least the reasons set forth above with respect to claim 15.

**Conclusion**

In view of the above remarks, the Applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge Deposit Account No. 08-2025, under Order No. 200205355-1 from which the undersigned is authorized to draw.

Respectfully submitted,

I hereby certify that this correspondence is being electronically filed with U.S. Patent and Trademark Office via electronic filing.

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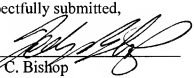
By 
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